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## NTE2033 Integrated Circuit Non-Inverting Transistor Array, Low Input Active

**Description:**

The NTE2033 is a non-inverting transistor array, which is comprised of four NPN darlington output stages and PNP input stages. This device is low level input active driver and is suitable for operation with TTL, 5V C-MOS and 5V Microprocessor which have sink current output drivers.

**Features:**

- Output Current: 1.5A Max.
- High Sustaining Voltage: 50V Min.
- Low Level Active Inputs
- TTL and C-MOS Compatible Inputs
- Standard Supply Voltage
- Two V<sub>CC</sub> Terminals V<sub>CC1</sub>, V<sub>CC2</sub> (Separated)

**Absolute Maximum Ratings:** (T<sub>A</sub> = +25°C unless otherwise specified)

Supply Voltage, V <sub>CC</sub> .....	-0.5 to 10V
Output Sustaining Voltage, V <sub>CE(sus)</sub> .....	-0.5 to +50V
Output Current, I <sub>OUT</sub> .....	1.5A
Input Current, I <sub>IN</sub> .....	-10mA
Input Voltage, V <sub>IN</sub> .....	-0.5 to +30V
Clamp Diode Reverse Voltage, V <sub>R</sub> .....	50V
Clamp Diode Forward Current, I <sub>F</sub> .....	1.5A
Common Terminal Current, I <sub>COM</sub> .....	3.0A
GND Terminal Current, I <sub>GND</sub> .....	5.0A
Power Dissipation, P <sub>D</sub> .....	2.7W
Operating Temperature Range, T <sub>opr</sub> .....	-40° to +85°C
Storage Temperature Range, T <sub>stg</sub> .....	-55° to +150°C

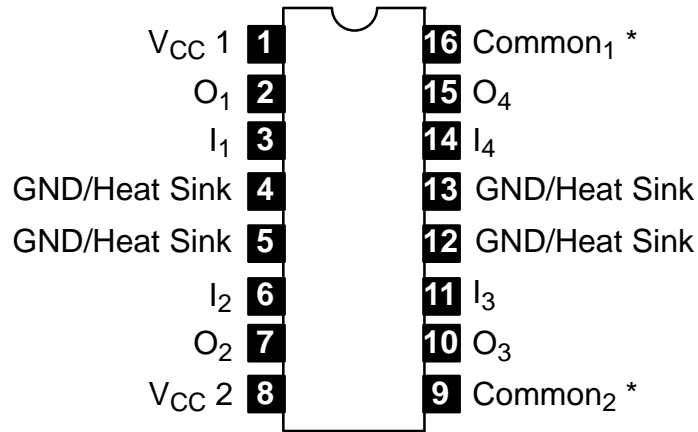
**Recommended Operating Conditions:** (T<sub>A</sub> = -40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>		4.5	-	5.5	V
Output Sustaining Voltage	V <sub>CE(sus)</sub>		0	-	50	V
Output Current	I <sub>OUT</sub>		0	-	1.25	V
Input Voltage	V <sub>IN</sub>		0	-	25	V
Clamp Diode Reverse Voltage	V <sub>R</sub>		0	-	50	μA
Clamp Diode Forward Voltage	V <sub>F</sub>		0	-	1.25	A
Power Dissipation	P <sub>D</sub>		0	-	1.0	W

**Electrical Characteristics:** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
"H" Level Input Voltage	$V_{IH}$		$V_{CC}-1.6$	–	25	V
"C" Level Input Voltage	$V_{IL}$		0	–	$V_{CC}-3.6$	V
"H" Level Input Current	$I_{IH}$		–	–	10	$\mu\text{A}$
"L" Level Input Current	$I_{IL}$	$V_{CC} = 5.5\text{V}, V_{IN} = 0.4\text{V}$	–	-0.05	-0.36	mA
Output Leak Current	$I_{CEX}$	$V_{OUT} = 50\text{V}, T_A = +85^\circ\text{C}$	–	–	100	$\mu\text{A}$
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$	$V_{CC} = 4.5\text{V}, I_{OUT} = 0.7\text{A}$	–	1.3	1.8	V
Clamp Diode Reverse Current	$I_R$	$V_R = 50\text{V}$	–	–	50	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_F$	$I_F = 1.25\text{A}$	–	1.5	–	V
Supply Current	$I_{CC(ON)}$	$V_{CC} = 5.5\text{V}, V_{IN} = 0\text{V}$	–	8.5	12.5	mA/Gate
	$I_{CC(OFF)}$	$V_{CC} = 5.5\text{V}, V_{IN} = V_{CC}$	–	–	10	$\mu\text{A}$
Turn–ON Delay	$t_{ON}$	$V_{CC} = 5\text{V}, R_L = 43\Omega$	–	0.2	–	$\mu\text{s}$
Turn–OFF Delay	$t_{OFF}$	$V_{OUT} = 50\text{V}, C_L = 15\text{pF}$	–	5.0	–	$\mu\text{s}$

**Pin Connection Diagram**



**Note:** These pins are internally connected.

